Low-Voltage Back-Gated Atmospheric Pressure Chemical Vapor Deposition Based Graphene-Striped Channel Transistor with High-κ Dielectric Showing Room-Temperature Mobility > 11 000 cm^2/V·s

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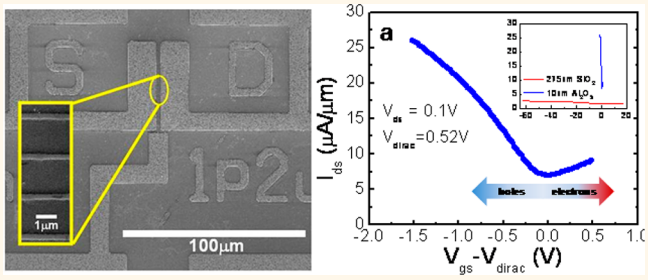
ABSTRACT Utilization of graphene may help realize innovative low-power replacements for III—V materials based high electron mobility transistors while extending operational frequencies closer to the THz regime for superior wireless communications, imaging, and other novel applications. Device architectures explored to date suffer a fundamental performance roadblock due to lack of compatible deposition techniques for nanometer-scale dielectrics required to efficiently modulate graphene transconductance (g_m) while maintaining low gate capacitance—voltage product ($C_{gs}V_{gs}$). Here we show integration of a scaled (10 nm) high-κ gate dielectric aluminum oxide (Al_2O_3) with an atmospheric pressure chemical vapor deposition (APCVD)-derived graphene channel composed of multiple 0.25 μm stripes to repeatedly realize room-temperature mobility of 11 000 cm^2/V·s or higher. This high performance is attributed to the APCVD graphene growth quality, excellent interfacial properties of the gate dielectric, conductivity enhancement in the graphene stripes due to low $t_{ox}/W_{graphene}$ ratio, and scaled high-κ dielectric gate modulation of carrier density allowing full actuation of the device with only $\pm$1 V applied bias. The superior drive current and conductance at V_{dd} = 1 V compared to other top-gated devices requiring undesirable seed (such as aluminum and poly vinyl alcohol)-assisted dielectric deposition, bottom gate devices requiring excessive gate voltage for actuation, or monolithic (nonstriped) channels suggest that this facile transistor structure provides critical insight toward future device design and process integration to maximize CVD-based graphene transistor performance.



KEYWORDS: graphene · striped channel · back-gate · high-κ · Al_2O_3 · mobility

Graphene, a two-dimensional allotrope of sp^2-bonded carbon, has generated tremendous interest across many disciplines of scientific research due to its unique electronic, mechanical, thermal, and chemical properties.[1] Room-temperature carrier mobility as high as 10 000 cm^2/V·s, small but controllable band gap, and very high cutoff frequency are some of the electronic properties of graphene that make it one of the key enabling materials for realizing low-power RF devices.[2−5] Many groups have previously reported on the performance of back-gated field effect transistors (FET) utilizing graphene synthesized by various techniques including exfoliation of highly ordered pyrolitic graphite, chemical vapor deposition, epitaxial growth on silicon carbide, and reduction of graphitic oxide.[6−9] The vast majority of back-gated transistor devices utilize thick (330 nm) silicon dioxide (SiO_2) as both isolation and gate dielectric to facilitate optical detection of the graphene channel albeit at the expense of very high switching voltage.[10] Attempts have been made to tailor the thickness of higher dielectric constant materials such as silicon

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nitride (Si_3N_4) or aluminum oxide (Al_2O_3) that still preserve the optical signature of graphene to improve electrostatic coupling.[11−15] Unfortunately, even the reduced thickness of these materials still requires high switching voltage because the dielectric thickness required for optical detection is at least an order of magnitude too large for low-power devices with reasonable gain (g_m/g_{ds}). In this work, we have demonstrated room-temperature mobility that is very high and at low-voltage operation by overcoming two important barriers to study graphene interaction with scaled high-κ dielectrics: (i) the difficulty of dielectric deposition on hydrophobic (untreated/pristine) graphene and (ii) lack of optical signature for graphene transferred to scaled high-κ dielectrics. The key to achieving this study is fabrication of back-gated devices on heavily doped silicon wafers where atomic layer deposition (ALD) was used to deposit scaled gate dielectric aluminum oxide (Al_2O_3) prior to aqueous-based transfer of continuous, uniform, and wafer-sized high-quality graphene synthesized by atmospheric pressure chemical vapor deposition (APCVD) such that the need for precise alignment of discrete source/drain contacts is eliminated (Figure 1). A comparable demonstration can be found in Han *et al.*'s work.[16] It is critically important to note that the graphene/dielectric interfacial quality is not impacted by the use of metal or polymer seed layers to facilitate growth of ALD high-κ dielectrics on hydrophobic graphene sheets, and transfer of our large (~6 cm × 6 cm) graphene sheets that cover the majority of the wafer surface circumvents the need for optical detection during subsequent lithography steps, whereas seeing the graphene is a requirement for randomly placed noncontinuous films.

RESULTS AND DISCUSSION

The Raman spectra shown in Figure 2 possess an I_{2D}/I_G ratio of 2−3 depending upon the substrate with little or no evidence of D peak signature (from graphene on Cu foil and Al_2O_3), thereby confirming the high quality of the double-layer graphene synthesized for use in this study. Moreover, the Raman map indicates a fairly uniform normalized I_{2D}/I_G peak intensity ratio over a large 40 μm × 40 μm area, while the accompanying optical image (of graphene on SiO_2) shows isolated higher contrast spots where the graphene sheet has wrinkled or folded during PMMA transfer from the Cu foil substrate. The dilute methane used during synthesis has been shown to suppress homogeneous nucleation density of graphene on copper foil and results in very large single-domain regions of graphene.[17−19] We expect that the majority of our device channels will easily fit within a single graphene domain, thereby reducing carrier scattering mechanisms at graphene grain boundaries and therefore affording higher mobility. The general broadening and appearance of satellite peaks near the conventional 1585 cm^{-1} G band in the specimens on SiO_2 and thin Al_2O_3 substrates are expected due to interaction with the substrate.[20,21]

Transfer characteristics normalized for both channel width and gate overdrive of representative devices with gate length of L_g = 2.4 μm on SiO_2 and Al_2O_3 substrates are shown in Figure 3a. Both devices exhibit p-type conduction typically seen in CVD-derived graphene films transferred from the growth substrate to the insulating substrate in aqueous solution media.[22] The device with scaled high-κ Al_2O_3 dielectric and striped graphene channel has an I_{ON}/I_{OFF} ratio of 3.75 and nearly 3000× higher normalized peak linear transconductance (g_m) than the SiO_2 specimen. These characteristics are rarely seen in back-gated devices and are attributed to the high quality of the graphene channel material, nonseeded high-κ dielectric, conductivity enhancement in the 250 nm width graphene stripes, and superior electrostatic coupling to the gate. Low-voltage actuation alleviates many of the

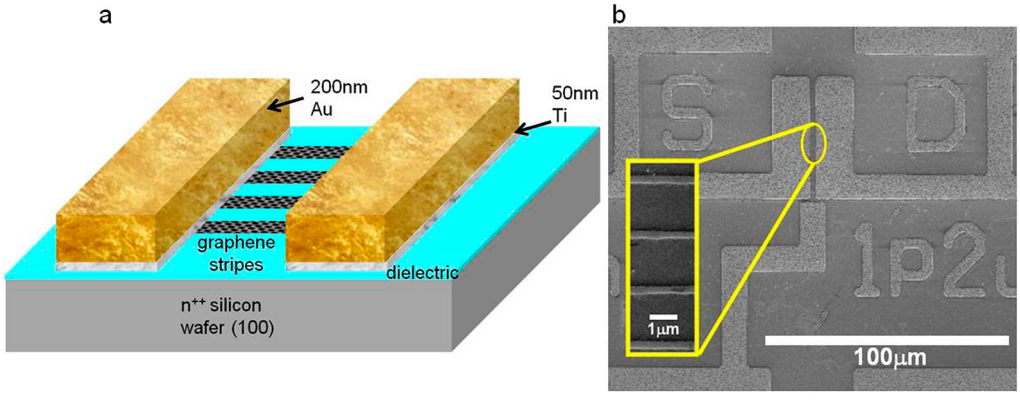

Figure 1. (a) Schematic of device after PMMA transfer of large 6 cm × 6 cm sheets of APCVD graphene to the Al_2O_3 dielectric surface, lift-off processing of the Ti/Au contact metal, and finally patterning of the graphene fins in the channel region. It is important to note that there is almost no contrast following PMMA removal, hence the need for large-area graphene over the 100 mm wafer to ensure a statistically sound data set. (b) Scanning electron micrograph (SEM) of a representative device. The inset shows sub-micrometer fin structures of graphene coated with photoresist for clarity.

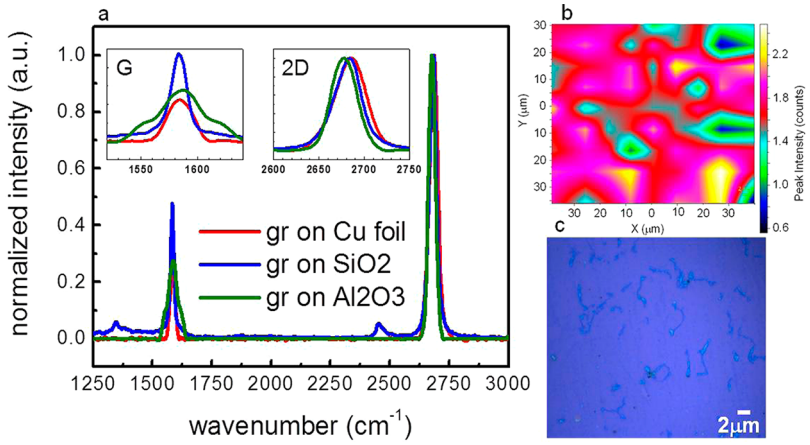

Figure 2. (a) Raman signatures of graphene films on copper foil and after transfer to the dielectric coated substrate. It was noted that a much higher attractive force existed between graphene and the Al_2O_3 substrate compared to SiO_2 during transfer from the final DI water rinse to the host substrate. Specifically, the graphene sheet could be "repositioned" on the SiO_2 substrate as it glided over the interfacial water layer, whereas the graphene irrevocably "stuck" to the Al_2O_3 surface upon contact. (b) Large-area Raman mapping of the I_{2D}/I_G intensity ratio indicates continuous and relatively uniform graphene on SiO_2 over very large areas. This criterion was especially important for this study due to the lack of optical contrast between graphene and the thin Al_2O_3 dielectric. (c) Zoomed-in optical image of graphene after transfer to SiO_2 substrate showing wrinkled and folded regions that give rise to anomalies in the Raman map.

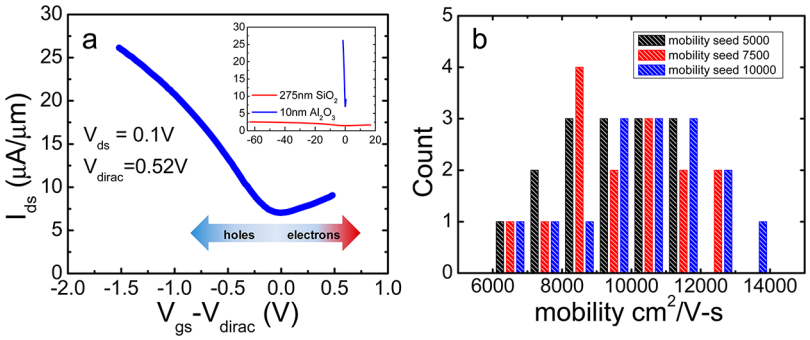

Figure 3. (a) Width-normalized I_d-V_g plot for the back-gated device on a thin Al_2O_3 dielectric with SiO_2 device shown in the inset. The 0.25 μm graphene stripes collectively exhibit an excellent I_{ON}/I_{OFF} of 3.75. Electron conduction is severely inhibited in these devices due to heavy p-type doping. Typical gate leakage current was <10 nA over the range of V_{gs} shown with breakdown occurring between 2.5 and 3 V V_{gs}. The inset shows the dramatic improvement in gate control from adopting the scaled gate dielectric. (b) Histogram of extracted mobility values from top-performing devices across a four-wafer die using three different seed values for regression analysis to simultaneously fit intrinsic carrier concentration, mobility, and contact resistance.

well-known parasitic fringing field issues present in ultrathin body MOSFETs.[23] It is also worth noting that this device architecture is particularly effective in maintaining high mobility due to screening of coulomb and phonon scattering by the high-κ dielectric and double-layer graphene, respectively.[24,25] Patterning the channel into fins in the quarter micrometer regime or smaller has been proposed as a means to enhance double-layer graphene's small band gap while maintaining excellent phonon-limited mobility as opposed to many nanoribbon-based device demonstrations that suffer significant mobility degradation due to edge scattering.[4,26,27] Recent reports have also shown that 0.5−3 μm wide graphene stripes experience up to 40% conductivity enhancement at the edges with degradation occurring at smaller widths due to the onset of carrier scattering from the graphene edges.[28] This effect has likely gone unnoticed in other reports of graphene channels patterned into sub-micrometer dimensions because the action of the fringing field to enhance edge conductivity manifests itself most effectively for a dielectric thickness to graphene width ratio (t_{ox}/W_{ch}) $\ll$ 1.[29] Hence, our choice of striped channel architecture and dimension coupled with a very thin dielectric is ideally suited to take advantage of edge conductivity enhancement without suffering edge scattering mobility degradation. Figure 3b shows a mobility (mobility data are obtained by overall fitting of I_dV_g data) histogram from 15 top-performing devices across the wafer. Transfer characteristics at V_{ds} = 1 V normalized for both channel width and gate overdrive shown in Figure 4 indicate a peak g_m/I_{drive} ratio that surpasses even the best top-gated devices with seeded deposition ALD films while still maintaining an I_{ON}/I_{OFF} ratio > 3.[30] As seen in the I_dV_d plot (Figure 4b), the unique device architecture enables significant

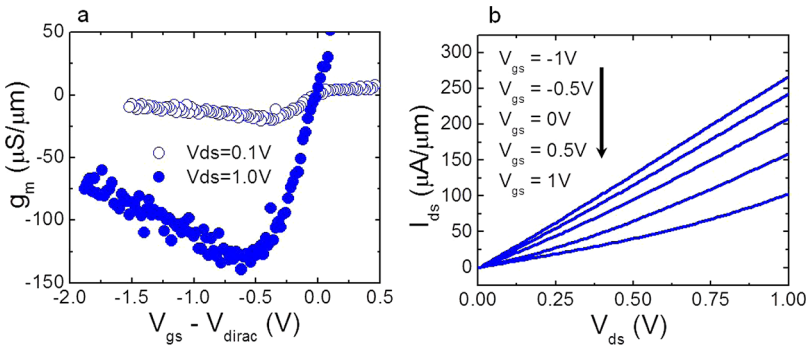

Figure 4. (a) Comparison of width-normalized transconductance for V_{ds} = 0.1 and 1 V conditions highlighting the ease of switching the device state at a fraction of gate voltage typically required for back-gated FETs. (b) Output characteristics (I_dV_d) indicate the device retains an appreciable I_{ON}/I_{OFF} ratio for V_{ds} = 1 V. It is important to note that the combined peak g_m of ~140 μS/μm, I_d^{sat} of >250 μA/μm, and I_{ON}/I_{OFF} ratio of >2.5 outstrip any of the seeded ALD dielectric growth techniques presented in ref 25.

drive current modulation for low 1 V system supply voltage (V_{dd}) and implies a room-temperature dc peak gain (g_m/g_{ds}) of 1.3, which is extremely difficult to achieve for FET demonstrations utilizing 1 order of magnitude larger back-gate voltage. A widely accepted model was used to extract effective mobility based on total device resistance.[31,32] The intrinsic (sheet) carrier concentration of ~1.42 × 10^{12} cm^{-2} and contact resistance that varies between 70% and 80% of the total device resistance (depending upon the back-gate voltage) is quite reasonable and in agreement with the mobility model used. For the Al_2O_3-deposited wafer, we examined several gate lengths to ascertain the changing nature of both channel and contact resistance inherent in a back-gated device architecture. Extrapolation of transfer length and contact resistivity gave values of 2.25 μm and 2.23 × 10^{-4} Ω·cm^2, respectively. This large contact resistivity is attributed to a residual photoresist layer present on the graphene/metal interface generated during lift-off processing of the source and drain electrodes since no descum was done prior to metal deposition. Recent reports indicating graphene−metal contact resistance reduction of more than 1000× *versus* untreated surfaces by oxygen plasma removal of residual surface contamination imply that the drive current of our device could be significantly increased by addressing this processing issue.[33] It is important to note that while carrier injection is certainly hampered due to S/D contact resistance, the graphene−dielectric interface suffered no such issues based on our integration scheme and therefore maintains high mobility for the device.

CONCLUSIONS

In conclusion, we have detailed a simple integration scheme utilizing a pristine scaled (10 nm) high-κ Al_2O_3 dielectric to fabricate a high-performance APCVD-derived graphene back-gated striped channel FET. The combined I_{ON}/I_{OFF} ratio of >3 and effective mobility of >11 000 $cm^2/V\cdot s$ indicate the use of pristine ALD dielectrics surpasses deposition methods that require metal/polymer/oxide seeding or surface functionalization typically employed for top-gated transistor architectures. There are several optimizations that can significantly improve the performance of graphene transistors of this type. Specifically, the I_{ON}/I_{OFF} ratio could be enhanced by more than 25× by employing lithographic techniques such as those utilized to generate Intel's 22 nm offering, the Tri-Gate, to pattern graphene stripes in a reliable manufacturable process that maintains excellent line edge roughness to mitigate the edge disorder mobility impact alongside congruent scaling of the gate dielectric to maintain the appropriate t_{ox}/W_{ch} ratio that preserves edge conductivity enhancement.[34,35] Additionally, reduction of contact resistance to values reported in ref 28 would translate to >5× higher drive current. Further reduction of the dielectric thickness below 5 nm is very feasible and would consequently scale the operation voltage for our device to less than 1 V V_{dd}. Other integration schemes that utilize buried gate architectures to allow for channel last processing, three-dimensional transfer techniques to increase effective channel width, or substrate engineering to modify residual strain/band gap could also enhance gate control and scalability of high-speed graphene transistors.

METHODS

At the beginning, large-area graphene films with low defectivity were synthesized on copper foils (25 μm thickness, 99.98% purity from Alfa Aesar) in a commercially available three-zone tube furnace with customized gas delivery. After surface cleaning in standard solvents, rinsing in deionized water, and drying with nitrogen, the copper foil was loaded into the tube furnace and annealed at atmospheric pressure in an argon/hydrogen

(Ar/H_2) mixture for 30 min at 1050 °C. Following this surface reduction anneal, 500 ppm methane in argon was introduced in place of pure argon for 15−30 min without changing temperature. After growth completion, the sample was pushed out of the hot zone to rapidly quench to room temperature under Ar/H_2 ambient before removing from the furnace. The cooling rate was not measured nor was it specifically controlled to alter the growth. We estimate that the cooling rate is on the order of 300 °C/min from the peak growth temperature of 1000 °C down to 50 °C, whereupon the cooling rate decreases. Raman data were acquired using a 532 nm laser line in a Horiba LabRAM HR unit before and after poly methyl methacrylate (PMMA)-based transfer of the graphene to heavily doped Si wafers coated with either 275 nm thermally grown silicon dioxide (SiO_2) or 10 nm ALD-deposited aluminum oxide (Al_2O_3). The SiO_2 was grown by a dry/wet/dry oxidation sequence in a tube furnace, while Al_2O_3 was grown *via* atomic layer deposition using a trimethyl aluminum precursor and H_2O reactant at 200−250 °C with a deposition rate of ∼1 Å/cycle. After solvent removal of PMMA, the wafers were exposed to a nitrogen/hydrogen gas mixture at 450 °C for 10 min to remove any additional PMMA residue and promote photoresist adhesion. Contact mask based liftoff lithography was utilized to pattern 50/200 nm Ti/Au source/drain contacts deposited *via* e-beam evaporation. Finally, a second mask was used to pattern graphene stripes and thus define the channel regions upon exposure to a short-duration O_2/Ar reactive ion etch (Figure 1).

Conflict of Interest: The authors declare no competing financial interest.

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